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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
TESSERA 3.0-306 II CIP I	

Application Number	Filed
10/783,314-Conf. #7827	February 20, 2004

First Named Inventor: Michael Warner, Lee Smith, Belgacem Haba, Glenn Urbish, Masud Beroz, and Teck-Gyu Kang

Art Unit	Examiner
2826	B. P. Sandvik

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant /inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 38,253
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

Signature

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Typed or printed name

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August 10, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of 1 forms are submitted.

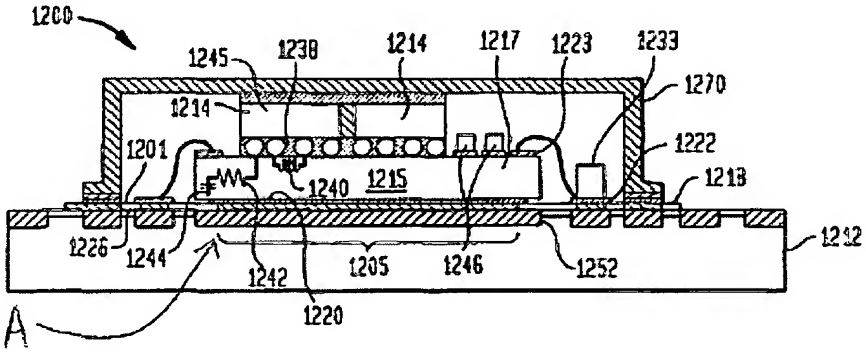
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: August 10, 2006 Signature: _____ (Daryl K. Neff)

The final Office Action rejected all claims as obvious over U.S. Pat. Pub. No. 2003/0001252 to *Ku* et al. ("*Ku*") in view of U.S. Pat. No. 6,657,296 to Ho et al. ("*Ho*"), or over *Ku*, *Ho* as combined with other references.

The invention recited in claim 2 resolves a problem of dissipating heat from a package including vertically connected chips to a circuit panel. Independent claim 2 recites an assembly including a circuit panel in which a flowable thermally conductive material connects a rear surface of one of the vertically connected chips to a mounting surface of a thermally conductive element included in the circuit panel. The invention of claim 2 achieves superior heat transfer through the direct connection provided between the chip's rear surface and the thermal element of the circuit panel by the flowable thermally conductive material. An example of this distinguishing feature of the interconnection is described at paragraphs 0070 -0080 of the Specification and is illustrated where marked by the undersigned at "A" in applicant's FIG. 17 below.

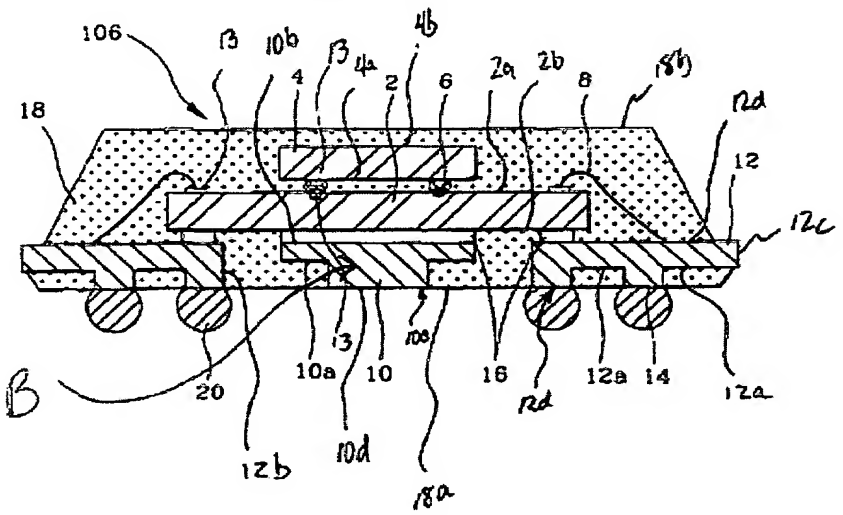
FIG. 17



The invention recited in claim 2 is clearly distinguished from the combination of *Ku* and Ho. *Ku* (FIGS. 4A through 5B) merely illustrates a conventional arrangement in which a chip's rear surface is attached to a "chip mounting plate 10" of the *package*, as seen in *Ku*, FIG. 4B where marked

"B" by the undersigned. The chip mounting plate is an element of the package, not of the circuit panel.

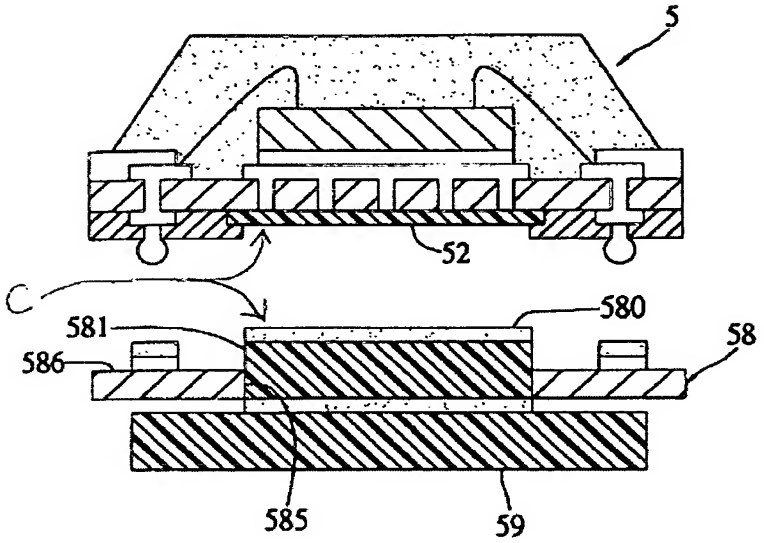
FIG. 4B



Clearly, The packaged chip of *Ku* requires additional elements to thermally connect the packaged chip to a thermally conductive element of a circuit panel.

In *Ho*, the rear surface of the lower chip is mounted to a "die attach region" 202 (FIG. 1), not to a thermally conductive element of a circuit panel. The die attach region 202, in turn, is thermally connected to a "thermal pad" 22 by way of "thermal vias 205". However, heat transfer is hindered by the substrate 20, through which the vias 205 must pass. As further illustrated in FIG. 5, as shown where marked "C" by the undersigned, only the thermal pad (52) is connectable to a heat sink 581 in a circuit board (by way of solder paste 580).

FIG. 5



Summarizing, in the invention recited in claim 2 the rear surface of a chip is connected to a thermal element of a circuit panel directly via a flowable thermal medium. By contrast, in the combination of *Ku* and *Ho* a series of different elements, a die attach region 202, thermal vias 205, thermal pad 52 and solder paste 580 are required to thermally connect the rear surface of a chip to a thermal element of the circuit panel. The elements recited in claim 2 are not present in the combination of *Ku* and Ho.

Moreover, none of the other cited references, either alone or in combination, teach or suggest the features of the invention recited in claim 2. *Hofstee* et al. (U.S. Patent Publication No. 2002/0074668) merely illustrates a multi-chip package 200 (FIG. 2) which includes a heat spreader 220, the heat spreader being separated from the chips of the module by both vertical thermally conductive elements 226 and two layers of lateral thermally conductive elements 224, 228. In addition, in *Tsai* et al. (U.S. Patent Publication No. 2004/0041249) the chip package includes a thin copper plate 27 sandwiched between two layers of adhesive 26, 52, one of which (26) attaches the

plate to a lower surface 14 of the package substrate 12. Again, this structure does not meet the language of a *flowable conductive material spacing* the rear surface from the mounting surface of a thermally conductive element *of the circuit panel*.

Reconsideration and withdrawal of the rejections is respectfully requested.